Hamed Abnavi

Semiconductor Device Engineer – Device Physics and Design
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Profile

PhD researcher with 8+ years of experience in semiconductor devices at the University of Twente, specializing in MOSFET design and modeling, TCAD simulation, and power-switch architectures across Si, SiC, and GaN technologies. Experienced across the device development cycle, including physics-based design, process and circuit simulation, optimization, fabrication-oriented design, and electrical characterization. Additional experience includes thin-film and perovskite solar cells, as well as oxide-based devices such as OxRAM memories.

Technical Skills

Device & Process Simulation	Silvaco VictoryDevice & VictoryProcess, Sentaurus TCAD
Circuit Simulation	PSpice, Silvaco Mixedmode, Cadence Virtuoso
Modelling & Analysis	MATLAB, parameter extraction, device modeling, characterisation
Technologies	Si, SiC, GaN, Perovskite materials; **MOSFET, HEMT, Diode, Nanosheet FET, thin-film solar cells, photodetectors, OxRAM memories**
Research Methods	Device engineering, RESURF design, $R_{\text{on,sp}} \cdot BV$ trade-off, electrical measurement and characterisation

Professional Experience

PhD Researcher – Power Semiconductor Devices 2023–Present *(expected: 28th Feb. 2027)*
University of Twente, The Netherlands

- Designed and optimized power semiconductor device architectures (trench MOSFETs, bidirectional switches) using physics-based TCAD simulation in Silvaco VictoryDevice and Sentaurus.
- Developed a novel RESURF accumulation-mode trench MOSFET concept as a bidirectional switch (up to 4× improvements in $BV \cdot R_{\text{on,sp}}$), resulting in a first-author publication in *IEEE Transactions on Electron Devices* (2025).
- Characterized fabricated Si devices (transfer/output characteristics, breakdown, parameter extraction) and benchmarked against industrial reference devices from NXP Semiconductors.
- Supervised MSc thesis work on simulation and modeling of GaN bidirectional HEMT devices.
- Conducting ongoing research on nanosheet FET architectures and electrostatic scaling limits for advanced technology nodes.

MSc Researcher – Micro- and Nanoelectronic Devices 2018–2021
Amirkabir University of Technology (Tehran Polytechnic), Tehran, Iran

- Designed, simulated, fabricated, and optimized perovskite solar cells and photodetectors.

- Fabricated triple-cation perovskite solar cells with carbon-based electrodes, achieving a 14% power conversion efficiency and an approximately 30% improvement over conventionally fabricated devices.
- Simulation study on electron/hole transport layers published in *Optical Materials* (2021, 73 citations).

Education

PhD – Power Semiconductor Devices 2023–Present
University of Twente, The Netherlands

MSc – Micro- and Nanoelectronics Devices 2018–2021
Amirkabir University of Technology (Tehran Polytechnic), Iran

BSc – Electrical Engineering, Control Systems and Robotic 2013–2018
VRU, Iran

Languages

English; Fluent Dutch; A2, in progress Persian; Native

Selected Publications & Awards

Journal Articles

H. Abnavi, C. Steenge, J.W. Berenschot, N.R. Tas, R.J.E. Hueting, "A New Silicon Accumulation-Mode Trench Bidirectional Switch," *IEEE Transactions on Electron Devices*, 2025. *(Citations: 1)*

H. Abnavi, D.K. Maram, A. Abnavi, "Performance Analysis of Several Electron/Hole Transport Layers in Thin Film $MAPbI_3$-Based Perovskite Solar Cells: A Simulation Study," *Optical Materials*, vol. 118, 111258, 2021. *(Citations: 78)*

Conference Papers

H. Abnavi et al., "Accumulation-Mode SiC Trench MOSFET," *Oral presentation, 17th International Seminar on Power Semiconductors (ISPS)*, 2025.

H. Abnavi et al., "Numerical Approach on Modeling of Perovskite Solar Cells Based on Coupled Ion Vacancy and Charge Carrier Dynamics," *32nd ICEE*, 2024.

Awards

MESA+ poster award 2025 – 3rd prize – Poster presentation: "Self-aligned 3D transistor technology in the MESA+ NanoLab" at MESA+ day 2025.

References

Available upon request.