

Hamed Abnavi

Semiconductor Device Engineer – Device Physics

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Profile

PhD researcher with 8+ years of experience in semiconductor devices at the University of Twente, specializing in MOSFET design and modeling, TCAD simulation, and power-switch architectures across Si, SiC, and GaN technologies. Experienced across the device development cycle, including physics-based design, process and circuit simulation, optimization, fabrication-oriented design, and electrical characterization. Additional experience includes thin-film and perovskite solar cells, as well as oxide-based devices such as OxRAM memories.

Education

PhD, Electrical Engineering – Semiconductor Devices 2023–Present (*expected: 28 Feb. 2027*)

University of Twente, Enschede, The Netherlands

Dissertation: Accumulation-mode bidirectional switch farm for energy efficient battery chargers.

Supervision group: dr.ir. R.J.E. Hueting, dr.ir. N.R. Tas, and ing. J.W. Berenschot

Summary: During my PhD, I focused on the design and engineering of novel accumulation-mode MOSFETs and bidirectional power switches for applications such as battery protection. My research involved the development of advanced device architectures, including vertical trench MOSFETs and nanosheet power FETs, with an emphasis on TCAD simulation, device optimization, and performance engineering. My work also included designing devices for fabrication at the MESA+ Institute, followed by the electrical characterization and laboratory measurements of the fabricated devices to validate their performance.

MSc, Electrical Engineering – Micro- and Nanoelectronic Devices

2018–2021

Amirkabir University of Technology (Tehran Polytechnic), Tehran, Iran

Thesis: Design, Simulation, and Fabrication of Perovskite Solar Cells and Photodetectors

Summary: My MSc research focused on the design, simulation, and optimization of novel thin-film perovskite solar cells through materials engineering to enhance device efficiency. This work was followed by the fabrication of triple-cation perovskite solar cells with carbon-based electrodes, achieving a power conversion efficiency of 14%, representing an approximately 30% improvement over conventional fabricated devices. My research also involved thin-film engineering, numerical modeling, and device optimization, resulting in several publications and a successful completion of my master's degree.

BSc, Electrical Engineering – Control Systems and Robotics

2013–2018

VRU, Kerman, Iran

Thesis: Designed the PCB and electronic circuit for a fully automated temperature and humidity controller with SMS-based remote monitoring and control.

Summary: Designed, programmed, and implemented a fully automated temperature (LM35) and humidity controller with SMS-based remote control. The project involved circuit and PCB design in Proteus, programming an ATmega32 microcontroller in C, PCB fabrication, electronic assembly, and system testing.

Research Experience

PhD Researcher, Power Semiconductor Devices

2023–Present

Power electronics / EEMCS, University of Twente, the Netherlands

- Designed and optimized power semiconductor device architectures (trench MOSFETs, bidirectional switches) using physics-based TCAD simulation in Silvaco VictoryDevice and Sentaurus.
- Developed a novel RESURF accumulation-mode trench MOSFET concept as a bidirectional switch, resulting in a first-author publication in *IEEE Transactions on Electron Devices* (2025).
- Characterized fabricated Si devices (transfer/output characteristics, breakdown, parameter extraction) and benchmarked against industrial reference devices from NXP Semiconductors.
- Supervised MSc thesis work on simulation and modeling of GaN bidirectional HEMT devices.
- Conducting ongoing research on nanosheet FET architectures and electrostatic scaling limits for advanced technology nodes.

MSc Researcher, Micro- and Nanoelectronic Devices

2018–2021

Amirkabir University of Technology (Tehran Polytechnic), Tehran, Iran

- Designed, simulated, fabricated, and optimized perovskite solar cells and photodetectors.
- Simulation study on electron/hole transport layers published in *Optical Materials* (2021, 73 citations).

Teaching and Mentoring Experience

- Daily supervisor, MSc thesis project on simulation and modeling of GaN bidirectional HEMT devices, University of Twente (2025–2026).
- Organized and supervised a three-month undergraduate project (MOD7A) for up to 24 students annually, covering TCAD simulation of photodiodes and MOSFETs, electrical characterization of fabricated devices, technical mentoring, and final report assessment.
- Teaching Assistant for the Power Semiconductor Devices course (annual appointment).
- Daily supervisor, BSc thesis project on simulation of GaN HEMT devices, University of Twente (2023).

Publications

Journal Articles

1. **H. Abnavi**, C. Steenge, J.W. Berenschot, N.R. Tas, R.J.E. Hueting, “A New Silicon Accumulation-Mode Trench Bidirectional Switch,” *IEEE Transactions on Electron Devices*, 2025. (Citations: 1)
2. **H. Abnavi** et al., “Performance Analysis of Several Electron/Hole Transport Layers in Thin Film MAPbI₃-Based Perovskite Solar Cells: A Simulation Study,” *Optical Materials*, vol. 118, 111258, 2021. (Citations: 76)

Conference Papers

1. **H. Abnavi** et al., “Accumulation-Mode SiC Trench MOSFET,” Oral presentation, *17th International Seminar on Power Semiconductors (ISPS)*, 2025.
2. **H. Abnavi** et al., “Numerical Approach on Modeling of Perovskite Solar Cells Based on Coupled Ion Vacancy and Charge Carrier Dynamics,” *32nd Iranian Conference on Electrical Engineering (ICEE)*, 2024.

3. Co-author, “Numerical and Computational Study on Compressive Strain Effect in Perovskite Solar Cells,” *32nd Iranian Conference on Electrical Engineering (ICEE)*, 2024.
4. Co-author, “Impedance Evaluation of Plasmonic Nano Dipole Antennas Based on Guided TE Mode,” *32nd Iranian Conference on Electrical Engineering (ICEE)*, 2024.
5. Co-author, “TDMA-Based Numerical Approach on Modeling of Charge Carrier Transport and Ion Vacancy Motion in Perovskite Solar Cells,” *32nd Iranian Conference on Electrical Engineering (ICEE)*, 2020. (Citations: 12)

Manuscripts in Preparation / Under Review

- Several additional publications (first-author and co-author) are currently under revision or in preparation.

Awards and Honors

- 3rd Prize, MESA+ Poster Award, for “Self-Aligned 3D Transistor Technology in the MESA+ NanoLab,” MESA+ Day, 2025.

Technical Skills

Device & Process Simulation	Silvaco VictoryDevice & VictoryProcess, Sentaurus TCAD
Circuit Simulation	PSpice, Silvaco Mixedmode, Cadence Virtuoso
Modelling & Analysis	MATLAB, parameter extraction, device modeling, characterisation
Technologies	Si, SiC, GaN, Perovskite materials; MOSFET, HEMT, Diode, Nanosheet FET, thin-film solar cells, photodetectors, OxRAM memories
Research Methods	Device engineering, RESURF design, $R_{on,sp} \cdot BV$ trade-off, electrical measurement and characterisation

Languages

English; Fluent Dutch; A2, in progress Persian; Native

References

Available upon request.